UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,853	01/31/2001	Tony San	ALTRP054/A574	3570

51501 7590 01/04/2006

BEYER WEAVER & THOMAS, LLP
ATTN: ALTERA
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,853	SAN ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-15, 41-44* is/are allowed.

6)☒ Claim(s) *16,17,19-21 and 37-40* is/are rejected.

7)☒ Claim(s) *18 and 22-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-44 were examined.

2. Claims 18, 22-36 are objected.

3. Claims 16, 17, 19-21, 37-40 are rejected.

4. Claims 1-15, 41-44 is allowed.

Section I: Non-Final Rejection (4th Office Action)

Joint Inventors Common Ownership Presumed

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 37-40 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. No clear definition, at least arithmetically, of the decimation factor.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 16, 17, 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Baicher et al.,("Learning About Digital Signal Processing Using Spreadsheets and Simulation Software" 1996) (hereafter Baicher). Baicher discloses a digital signal processing (DSP) method with spreadsheets (abstract).

Claim 16. A method of compiling a filter having a selected filter spectral filter spectral response, comprising: providing a first set of filter coefficients corresponding (pg. 42, right column 2nd bullet statement) to the filter spectral response; providing an expected filter spectral response based in part upon the first set of filter coefficients (pg. 42, right column 2nd bullet statement); comparing the desired filter spectral response to the expected filter spectral response; estimating an implementation output file (the

suggestion of a output file relating to the filter response; pg. 47, figure 5 and pg. 44, figure 2 (plurality of frequency responses)).

Claim 17. A method as recited in claim 16, wherein when the expected filter spectral response (pg. 42, right column 2nd bullet statement) is substantially the same as the selected filter spectral response, then the first set coefficients is a second set of filter coefficients.

Claim 19. A method as recited in claim 18, wherein the filter is finite impulse response (FIR) filter (pg. 42, right column 2nd bullet statement).

Claim 20. A method as recited in claim 16, wherein the filter coefficients are FIR coefficients, (pg. 43, left column, equations 3-4) and wherein the selected spectral response is a FIR filter spectral response, and wherein the expected filter spectral response is an expected FIR filter spectral response (pg. 43, left column, lines 1-12), and wherein the desired filter implementation output file is a desired FIR filter implementation output file (pg. 47, figure 5 and pg. 44, figure 2 (plurality of frequency responses)).

Claim 21. A method as recited in claim 21, further comprising: when the first set of FIR filter coefficients is a set of floating-point (pg. 42, left column, 2nd paragraph, lines 6-

7) FIR filter coefficients, converting the set of floating-point FIR filter coefficients to a set of fixed-point FIR filter coefficients.

Allowable Subject Matter

10. Claims 1-15, 41-44 is allowed

11. Claims 18, 22-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitation of the base claim and any intervening claims.

12. The following is an examiner's statement of reasons for allowance:
While Eminoglu et al. "A CAD Environment for Digital Filters Using A VerilogHDL Based Functional Bit-Serial Compiler" a filter compiler, comprising: a filter coefficient generator arranged to provide a first set of filter coefficients corresponding to a filter spectral response; a filter spectral response simulator coupled to the filter coefficient generator for providing an expected filter spectral response based in part upon the first set of filter coefficients (claim 1); Baicher et al.,("Learning About Digital Signal Processing Using Spreadsheets and Simulation Software" 1996) teaches a FIR compiler (claim 41), none of these references, taken either alone or in combination, with the prior art of record disclose a serial compiler, including:

(claim 1) "a filter resource estimator coupled to the filter spectral response simulator for estimating an implementation cost of a filter, wherein a cost analysis is performed substantially in parallel with a performance analysis; and a filter compiler unit coupled to the filter resource estimator arranged to compile a filter implementation output file"

(claim 18) " a cost filter"

(claim 22) "converting the set of floating-point FIR"

(claim 26) "a MATLAB TESTBENCH model"

(claim 27) "a multi-rate FIR"

(claim 30) "filter symmetry"

(claim 41) "applying a first clock rule when an input data width is less than or equal to an interpolation factor; and applying a second clock rule when an input data width is greater than the interpolation factor".

While Baicher teaches a high speed digital processor with FIR filters neither Baicher or Eminoglu, taken either alone or in combination with the prior art of record, disclose filter resource estimators including decimating filters in combination with the

remaining elements and features of the claimed invention. It is for these reasons that the applicants' invention defines over the prior art of record.

13. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Section II: Response to Applicants' Arguments (3rd Office Action)

Oath

14. Applicants are thanked for addressing this issue. Objection is withdrawn by way of applicants' submission of the application data sheet as required by MPEP 602.01.

35 USC § 112 1st and 2nd

15. Applicants are thanked for addressing this issue. Rejections are withdrawn.

Claim Objections

16. Applicants are thanked for addressing this issue. Rejections are withdrawn.

Citation to Relevant Prior Art

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Mathworks Inc. "Student Edition of MATLAB" 1997. pgs.38,39, 256,257,335-345; teaches various aritmatatic tools for scientific experimentation and simulation.

- Bishop-R.H., "Modern Control Systems Analysis and Design Using MATLAB & SIMULINK" 1997. pg. 95-101,192-207,211-214: comprises a aritmatic simulation program.

- Eminoglu et al., "A CAD environnnent for digital filters using a VerilogHDL based functional bit-serial compiler" 1998. pg.91-94. 10th International Conference Monastir Tunisia (abstract). pg.1-2: This paper reports the development of a highly integrated CAD environment for area efficient implementation of digital filters using commercially available CAD tools. The environment establishes a plain interface between CADENCE (an IC design framework), MATLAB (a mathematical computation tool), and BITMAP (a new custom-developed filter compiler).

- "The Altera Advantage News and Views" May 1997. pg.1-31 teaches Altera's MAX programmable logic devices as well as their MAX +PLUS II compilers.

- "FIR Compiler MegaCore Function" Solution Brief 41, June 1999, ver.1 pg. 1-4 teaches a brief summary of the FIR compiler parameters and properties.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Leo Picard ((571) 272-3749). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

December 14, 2005

TS

Paul L. Rodriguez 12/27/05

Primary Examiner
Art Unit 2125